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Silicon on Insulator (SOI) Technology - SlideShare

For instance, 28 nm technology has requirement for wire width to be, say, minimum of 35 nm. But we can always draw wires with larger width like 100 nm, which can be the minimum wire width of 90 nm technology. And 100 nm width wires will have less resistance than 35 nm wires. So, technology is just a placeholder for minimum dimensions.

*Latchup In Cmos Technology The
Complementary
metal-oxide-semiconductor (CMOS,
pronounced "see-moss"), also known
as complementary-symmetry
metal-oxide-semiconductor (COS-*

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MOS), is a type of metal-oxide-semiconductor field-effect transistor (MOSFET) fabrication process that uses complementary and symmetrical pairs of p-type and n-type MOSFETs for logic functions. CMOS technology is used for constructing integrated ...

CMOS - Wikipedia

It is a technology developed by Canon ELTRAN (Epitaxial Layer TRANSfer) SOI Technologies 26. CMOS Fabrication by SOI Technology The subsequent steps for fabrication of CMOS are similar to Bulk Technology 27. Bulk vs SOI 28. CMOS in Bulk vs SOI technology 29. CMOS in Bulk vs SOI technology 30. Types of SOI Devices 31.

Radiation hardening - Wikipedia

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Latch-up characteristics are extremely important in determining product reliability and minimizing No Trouble Found (NTF) and Electrical Overstress (EOS) failures due to latch-up. This test method is applicable to NMOS, CMOS, bipolar, and all variations and combinations of these technologies.

How to fix setup violations - VLSI UNIVERSE

Radiation hardening is the process of making electronic components and circuits resistant to damage or malfunction caused by high levels of ionizing radiation (particle radiation and high-energy electromagnetic radiation), especially for environments in outer space (especially beyond the low Earth orbit), around nuclear reactors and particle accelerators, or during nuclear accidents or nuclear ...

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