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*Contents Acknowledgments vii Foreword ix
Preface xi The Boiled Frog 1 A Boiled Story 3
Root Cause Analysis 4 The "Verification
Complete" Milestone 5*

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operation of the testbench, which stimulates
the FPGA. The simulation process observes the
transformations and translations of signals
as they propagate through the FPGA from the*

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input pins and provides responses that eventually reach an output pin.

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