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EE 460M Digital Systems Design Using VHDL Lab Manual Problem 3: Synthesizing and implementing the BCD counter on the FPGA Use the code for the single digit BCD counter that you wrote in Problem 2a. Before you synthesize it and implement it on the board, you will have to modify your code a little bit.

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Authors: Charles H. Roth, Jr. - University of Texas, Austin; Lizy Kurian John - University of Texas, Austin Thomson Engineering. Written for an advanced-level course in digital systems design, DIGITAL SYSTEMS DESIGN USING VHDL integrates the use of the industry-standard hardware description language VHDL into the digital design process.

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2.21. 2.22. Unlike Clr, the output from the mux is only read on falling clock edges; therefore, adding C to the sensitivity list is not required for proper operation of the circuit. 2.23 (a) sel ...

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About Author. Charles Roth is Professor Emeritus in Electrical and Computer Engineering at the University of Texas at Austin, where he taught Digital Design for more than four decades. He is the author of Fundamentals of Logic Design, which is in its sixth edition, and Digital Systems Design using VHDL, which is in its second edition.

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Written for an advanced-level course in digital systems design, DIGITAL SYSTEMS DESIGN USING VHDL integrates the use of the industry-standard hardware description language VHDL into the digital design process. Following a review of basic concepts of logic design in Chapter 1, the author introduces the basics...

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1.5. A static 1-hazard occurs when  $A = 0$ ,  $D = 0$ , and  $C$  changes. When  $C$  changes from 1 to 0;  $A'C$  also goes from 1 to 0. The hazard occurs because  $C'$  hasn't become 1 yet since it has to go ...

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