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Digital Design 101 |
DGLogic
View Test Prep - Fall
2016 Midterm 1 Practice
- Jaja from ENEE 244 at
University of Maryland,
College Park. ENEE244:
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Spring 2016 Midterm I 1.

(a) [16pt] Show how to
convert

ECGR2181 - Logic
Systems Design I - Exams
Course Objective : The
goal of this course is to
learn the basic principles
of digital design. The
course aims at enabling a
student to design small
digital systems for

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different applications
starting from abstract
specifications or
behavioral/structural
descriptions.

Fall 2013 - ECE238L:
Computer Logic Design
Start studying Digital
Logic Design Exam 1.
Learn vocabulary, terms,
and more with flashcards,
games, and other study
tools.

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Digital Logic Design
Midterm 1

EECS:1100 Digital Logic
Design Dr. Anthony D.
Johnson Student

Name_____ 3/14/18

Problem 1 3 points For
full credit, mark your
answers yes, no, or not
applicable for all offered
choices! 1.1 The bit
strings shown below are

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Utah State University
Engineering

valid representations of
negative numbers in the
eight-bit two's

Fall 2016 Midterm 1
Practice - Jaja -
ENEE244 Digital Logic...
Digital Logic I EE 2720-2
Midterm Examination
102 9 November 2011,
14:40 – 15:30 CST Exam
Rules Use only a pencil
or pen. No calculators of
any kind are allowed.

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Texting is out of the question. Alias Saila

Problem 1 (22 pts)

Problem 2 (22 pts)

Problem 3 (22 pts)

Problem 4 (12 pts)

Problem 5 (12 pts)

midterm design exam
unit 1 digital Flashcards -
Quizlet

Mar 1: Detailed
discussion of midsem
solutions. Role of don't

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cares in digital logic design, and various sources of don't cares.

Mar 2: Holi break : Mar 8: More on different kinds of don't cares, reasons why they arise, and how they can be exploited.

Digital Logic I EE 2720-2
Midterm Examination
Learn midterm design exam unit 1 digital with

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different sets of midterm
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flashcards on Quizlet.

Fall 2016 - ECE278:
Digital Logic Design
ICS 151 Digital Logic
Design, Spring Quarter
2006, Midterm Page 3
Q2: FSM Design [20
points] Design a state
diagram for a recognizer

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that recognizes an input sequence 11101. It has an input X and output Y.

The recognizer sets the output to 1 ($Y = 1$) for exactly one clock cycle if the last five values on the input X were 11101

Sample Final Exam
Solutions - uidaho.edu
Welcome to the Digital
Gate Logic (DGLogic)
System Web Site. This

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site currently manages 2
digital design courses:

Digital Design Logic 101
(EECS/CSE 31) and
Digital Design Logic Lab
101 (EECS/CSE 31L).

Relevant course material
will be referenced on this
site or the corresponding
EEE MessageBoard for
the current offering of the
course.

Spring 2006 - Donald

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Bren School of

Information and ...

Logic Circuits (630211)

Exams . Exams

(2019-2020) First

Semester: Quizzes . Quiz

1 Solution . Quiz 2

Solution . First Exam ...

Second Exam : Solution .

Exams (2018-2019)

Second Semester: Quiz .

Quiz Solution . First

Exam. First Exam:

Solution . Second Exam.

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Second Exam : Solution .
Final Exam. Final Exam :
Solution. Exams
(2018-2019) First ...

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Exam 1 Flashcards |
Quizlet

For the Love of Physics -
Walter Lewin - May 16,
2011 - Duration: 1:01:26.
Lectures by Walter
Lewin. They will make
you Physics.

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EECS:1100 Digital Logic
Design Dr. Anthony D.
Johnson Student

Name_____ 2/16/17

Problem 1 3 points For
full credit, mark your
answers yes, no, or not
applicable for all offered
choices! 1.1 The bit
strings shown below are

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valid representations of
negative numbers in the
four-bit two's

CS 151 SQ08 Digital
Logic Design

This is a lecture on
Digital Design,
specifically a review
before an exam.

Examples are given of
Kmaps and Boolean
Algebra. Lecture by
James M. Conrad at the

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University of North
Carolina at Charlotte.
Engineering

21 published for
Midterm only CS302
Digital Logic Design ...
Faculty of Engineering .
ELECTRICAL AND
ELECTRONIC
ENGINEERING
DEPARTMENT .
EENG115/INFE115
Introduction to Logic
Design Introduction

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Digital Logic
Design Midterm 1
to Logic Design/ Digital
Logic Design I - Midterm
Examination Question 2
(20 points): a) Find the
($r-1$) ' s and r ' s
complements of the
following numbers in the
indicated bases. (10

Faculty of Engineering -
faraday.ee.emu.edu.tr
EECE 256 Digital Logic
Design . Section 101/102
Term 1 - 2010/11. Final

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Exam in SRC A,
3:30-6:00, Tuesday Dec 7
th. Midterm Solution &
old final questions
posted. Exam covers
Chap

Logic Circuits (630211)
Exams
COE/EE 243 Digital
Logic Session 44; Page
1/5 Spring 2003 COE/EE
243 Sample Final Exam
From Fall 98 Solutions

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Show your work. Do
NOT use a calculator! 1.
(9 pts) Complete the
following table of
equivalent values.

Lecture 1 - Basic Logic
Gates | Digital Logic
Design | MyLearnCube
UNC- Charlotte ECGR
2181 - Fall 2009 - Logic
Systems Design I
Recitation - All Sections:
8:00 - 10:45 F,

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Woodward 125 ... Fall
2009 Midterm Exam

Solution: Link to
solution - Exam 1 MC;
Link to solution - Exam 1
Problems ... 9/18/09 -
Boolean Algebra, digital
gates ; Quiz 5 - 9/25/09 -
Minimizing SOP,
XNOR/NAND/NOR
logic gates; Quiz 6 -
10/2/09 ...

Digital Design: Midterm

Read Online
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Design Midterm 1
Exam Review – Kmaps,
Boolean Algebra
Prof. Hanna's book:
Introduction to Digital
Design Using Digilent
FPGA Boards - Block
Diagram/VHDL
Examples Unit 1:
Introduction to Logic
Circuits Lecture Notes -
Unit 1

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Midterm #1

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published for Midterm
only CS302 Digital Logic
& Design_ Muhammad
Ishfaq Page No.61 True
False Question No: 3

Please choose one The
values that exceed the
specified range can not
be correctly represented
and are considered
as_____ Overflow Carry
Parity Sign value

Question No: 4 Please

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choose one The 4-bit
2's complement
representation of “ -7 ”
is _____ 0111 1111 1001
...

UBC EECE 256 - Digital
Logic Design
Fall 2014 - ECE470/570:
Microprocessor-Based
System Design; Fall 2013
- Workshop: Digital
Circuit Design with
VHDL; Fall 2013 -

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ECE238L: Computer
Logic Design; Summer
2013 - ECE314: Signals
and Systems; Fall 2005 -
IEE146: Laboratory of
Digital Circuits (in
Spanish) Digital Library.
DSP/DIP cores;
Arithmetic Cores; Fall
2013 - Computer Logic
...

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bcd3a24f0](#)
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