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Solution

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## **Getting Started with Altera's DE2 Board**

### **Laboratory Exercise 1**

#### **Switches, Lights, and**

**Multiplexers** The purpose of this exercise is to learn how to connect simple input and output devices to an FPGA

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**chip and implement a circuit that uses these devices. We will use the switches SW 17 0 on the DE2-series board as inputs to the circuit.**

**VLSI ON NET: ALTERA DIGITAL LAB SOLUTIONS (DE1 Board)**

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**ECE 5760 deals with system-on-chip and embedded control in electronic design. The course was taught from 2006-2019 by Bruce Land, who is a staff member in Electrical and Computer Engineering. ECE 5760 thanks**

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**INTEL/ ALTERA for their donation of development hardware and software, and TERASIC for donations and timely technical support of their hardware.**

**Lab 1: Part II - Introduction to**

*Page 8/37*



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**DE2 and Nios II Assembly  
Terasic—DE2 board. ...  
=53&No=30. Used in all  
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## **Laboratory Exercise 1 - MWFTR**

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## **Altera De2 Labs Solution**

**This is my set of solutions to Altera's DE2 example labs. These were done as part of a course I took at university**

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**during the Fall of 2010. I am publishing this code because I found these labs challenging and had a hard time getting help on them.**

**Altera University Program -  
Digital Logic - Lab 1 Part 2**

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**Our tutorials are intended for self-study by students. The tutorials cover our FPGA boards, software tools, including the Quartus® CAD system, the Nios® II and ARM\* processors, and other topics.**

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Bing - PDFsDirNN.com  
The Verilog 1 Lab from Altera  
is a rather lengthy lab for a  
beginner lab. From my**



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**estimates, a student should take several hours per day to finish it. I highly recommend reading Altera's Verilog Laboratory Exercise 1 before reading this article as I will go quickly through the solutions. This lab contains 6 parts that**

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**cover mid level logic design.**

**ECE 5760 - Cornell University  
Lab 1: Part II - Introduction to  
DE2 and Nios II Assembly  
Description Preparation (1  
mark) In Lab (1 mark) Quiz (1  
mark) Description. The**

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**purpose of this lab is for you to gain familiarity with Assembly Language Programming, and the environment for programming the Altera Nios II processor at the assembly language level.**

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**Altera DE2 Board Resources for Students. click DE2 image above to view larger image.**  
**How to purchase a DE2 board.**  
**New DE1 info is here. New Camera and LCD info is here**

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**DE2 Design Examples DE2  
Clock is a clock/timer that  
uses the DE2's LCD to display  
the current time. A VHDL-  
based state machine is used  
to communicate with the LCD  
display controller.**

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stemmed from my childhood  
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**awe as it began to display a picture on screen.**

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Lab\_4\_ISR\_Debug.  
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**Fall semester 2010: HW 1  
(Due September 3, 2010) HW  
2 (Due September 24, 2010)  
HW 3 (Due October 15, 2010)  
Lecture Slides: Lecture 1 and  
Altera DE2 reference Altera  
DE2 Board User Manual.  
Lecture 2. Lecture 3. Lecture**



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## 4. Lecture 5

**GitHub - BenBergman/AlteraD  
E2Labs\_Verilog: My solutions  
to ...**

**The following laboratory  
exercises cover basic  
concepts such as switches,**

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**lights, and multiplexers, as well as common building blocks like arithmetic circuits, latches, registers, counters, and finite state machines.**

**FPGA Project: Verilog Lab 1:  
Altera DE2 Board - Basic**

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## **Verilog**

**Hey Everyone, Continuing the Altera University Program series with Lab 1 Part 2. The section continues with basic switch and LED capabilities, but focuses on Multiplexers (MUXs). As usual I ...**

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## **University - University Tutorials**

**Terasic is the world's leading designer and vendor. We offer expertise in FPGA/ASIC Design, Board Design and Layout, Device Drivers, and**

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**Altera Tutorials and Lab**

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## **Exercises - Scribd**

**altera digital lab solutions  
(de1 board) Laboratory**

**Exercise 1 Switches, Lights,  
and Multiplexers PART1:**

**PROGRAM: module part1(SW  
,LEDR); input [9:0]SW; output  
[9:0]L... SYSTEM VERILOG**

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## **PART-1**

**Terasic Inc. - Expertise in  
FPGA/ASIC Design  
- Cyclone II EP2C35F672 with  
~35,000 LEs - 8MB SDRAM,  
512K SRAM, and 4MB Flash -  
TV decoder, Ethernet, RS232,**

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## **and USB Host/Device**

**Terasic - Phased Out - Main  
Boards - Altera DE2 Board  
Getting Started with Altera's  
DE2 Board This document  
describes the scope of  
Altera's DE2 Development**



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**and Education Board and the supporting materials provided by the Altera Corporation. It also explains the installation process needed to use a DE2 board connected to a computer that has the Quartus R II CAD system**

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**installed on it. Contents:**

**University - Laboratory  
Exercises**

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development by creating an**

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**account on GitHub.**

**Digital Design DE2 FPGA Kit  
lab. solution · rsulh/Altera ...  
Last term I took a course that  
involved a lot of FPGA  
programming. We used  
Altera's DE2 development**

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**board as well as their example labs (Digital Logic and the first few Computer Organization labs). While the labs were quite enjoyable and very educational, it was a LOT of work compared to labs in other courses.**

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